Claims

[c1] A method of fabricating a field effect transistor (FET) having a metal gate structure, comprising:
forming a metal gate structure in an opening within a dielectric region formerly occupied by a sacrificial gate, said metal gate structure including:
a first layer including one or more materials selected from the group consisting of metals and compounds of metals, said first layer contacting a gate dielectric, the gate dielectric contacting a transistor channel region formed in a semiconductor region of a substrate; and
an overlying silicide layer overlying said first layer; and
forming a source region and a drain region on opposite sides of said metal gate structure.

[c2] The method of claim 1 wherein said step of forming said metal gate structure includes depositing a layer of silicon over said first layer, depositing a layer of metal over said layer of deposited silicon, and reacting said deposited silicon with said deposited metal to form said overlying silicide layer in a self-aligned manner.

[c3] The method of claim 2 wherein said step of forming said metal gate structure further includes forming an under-

lying layer of silicide at an interface between said first layer and said layer of deposited silicon.

[c4] The method of claim 3 wherein said first layer consists essentially of a single metal whose work function has a value at about the middle bandgap of silicon.

[c5] The method of claim 4 wherein said single metal is tungsten.

[c6] The method of claim 5 wherein said underlying layer of silicide consists essentially of tungsten silicide.

[c7] The method of claim 6 wherein said overlying silicide layer consists essentially of cobalt silicide.

[c8] The method of claim 6 wherein said overlying layer of silicide consists essentially of nickel silicide.

[c9] The method of claim 1 wherein said gate dielectric includes a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, and zirconium oxide.

[c10] The method of claim 1 wherein said opening in said dielectric region is lined with dielectric spacers, said dielectric spacers having been formed on sidewalls of said sacrificial gate.

[c11] The method of claim 10 wherein said dielectric spacers include L-shaped oxide spacers having sidewalls exposed at said opening and overlying nitride spacers.

[c12] A method of fabricating a field effect transistor (FET), comprising:
forming a sacrificial gate disposed between a pair of spacers over a semiconductor region of a substrate;
forming a source region and a drain region on opposite sides of said sacrificial gate;
forming a dielectric layer on said substrate having a top surface generally planar to a top of said sacrificial gate;
removing said sacrificial gate to form an opening between said pair of spacers, said opening extending to said semiconductor region;
forming a gate dielectric on said semiconductor region in said opening;
forming a first layer in said opening including at least one material selected from the group consisting of metals and compounds of metals;
depositing a layer of silicon on said first layer in said opening;
removing said dielectric layer and forming a second metal layer including a silicide-forming metal over said source region and said drain region and said layer of silicon; and

annealing said substrate to form a silicide from said silicide-forming metal, said silicide contacting said source region and said drain region and contacting said layer of silicon.

[c13] The method of claim 12 wherein said annealing also forms a silicide at an interface between said first metal layer and said layer of silicon.

[c14] The method of claim 13 wherein said silicide-forming metal includes at least one metal selected from the group consisting of cobalt, nickel, titanium and platinum.

[c15] An integrated circuit including a field effect transistor (FET) having a metal gate structure, comprising:
a gate formed in an opening within a dielectric region formerly occupied by a sacrificial gate, said gate including a first layer contacting a gate dielectric formed over a semiconductor region of a substrate, said first layer including a material selected from the group consisting of metals and metal compounds, said gate further including a silicide formed over said first layer; and
a source region and a drain region formed on opposite sides of said gate.

[c16] The integrated circuit of claim 15 further comprising a

silicide contacting said source region and said drain region.

[c17] The integrated circuit of claim 15 wherein said first layer consists essentially of a single metal whose work function has a value at about the middle bandgap of silicon.

[c18] The integrated circuit of claim 17 wherein said single metal is tungsten.

[c19] The integrated circuit of claim 15 wherein said overlying silicide layer consists essentially of a silicide of a metal selected from the group consisting of cobalt, nickel, platinum and titanium.

[c20] The integrated circuit of claim 15 wherein said gate dielectric includes a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, and zirconium oxide.